REMARKS/ARGUMENTS

The Applicant originally submitted Claims 1-28 in the application. In previous responses, the Applicant added Claims 29-30 and canceled Claims 23-29 without prejudice or disclaimer. In the present response, the Applicant has amended Claims 1, 22, and 30 solely in response to pending objections to these claims. No other claims have been added or canceled. Accordingly, Claims 1-22 and 30 are currently pending in the application.

I. Formal Matters and Objections

The Examiner has stated that the IDS submitted on July 29, 2010 has not been considered because the citation did not include the author. In response, the Applicant submitted an IDS on August 25, 2010 in which the author for the citation was included. Accordingly, the Applicant respectfully requests the Examiner to consider the citation.

The Examiner objected to Claims 1, 22, and 30 as containing informalities. In response, as noted above, the Applicant has amended these claims consistent with the Examiner's direction in the Office Action. Accordingly, the Applicant respectfully requests the Examiner to withdraw the objection to these claims and allow issuance thereof.

II. Rejection of Claims 1-22 an 30under 35 U.S.C. §103

The Examiner has rejected Claims 1-22 and 30 under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 5,737,631 to Trimberger (hereinafter "Trimberger") in view of an article entitled "Configurable Multiplier Blocks for use within an FPGA", 1998 by Haynes, *et al.*

(hereinafter "Haynes"), an article entitled "A Flexible LUT-Based Carry Chain for FPGAs", 2003 by Lodi, *et al.* (hereinafter "Lodi"), and U.S. Patent No. 7,176,713 to Madurawe (hereinafter "Madurawe"). The Applicant respectfully disagrees.

In paragraphs 12-11 on page 8 of the Office Action, the Examiner rejects previously presented dependent Claims 4-6, asserting that portions of Trimberger disclose configurable operators are configurable at a level of multi-bit values. This is incorrect. What this feature means is that each configurable operator can itself handle a multi-bit value and can be configured at that level. Operators can be, *e.g.*, ALU operators or multiply operators, *etc.* (*See*, *e.g.*, the beginning of the discussion of Fig. 3 on page 12 of the original specification.) Each operator of the present invention can be configured at this level.

Trimberger discloses an FPGA in which the level of configurability is at a gate level. That is, it is at a single bit level. In an FPGA, each bit is configured by the configuration information such that for any particular input, a certain output is reached. There is no concept of multi-bit operators. (*See* also, *e.g.*, the bottom of page 6 of the original specification which defines configurability.)

The Examiner refers to a multi-bit opcode. The opcode merely indicates that a particular RISA configuration is to be utilized. That is, it defines the instruction implemented by the RISA. The configuration itself in a conventional FPGA is carried out at a single bit level, and, moreover, is not implemented by the opcode.

In paragraph 18 at the bottom of page 9 and top of page 10 of the Office Action, the Examiner rejects previously presented dependent Claim 10 alleging Trimberger discloses that "configuration information which determines the nature of operations to be performed" is received

"from a field of an instruction defining a configurable data processing operation." Trimberger does not disclose this. Trimberger does not disclose that configuration information for configuring the FPGA comes from a configurable data processing instruction. Configuration of the FPGA in Trimberger is carried out using special configuration information during a reconfiguration process. It is clear from Trimberger that the configuration information is not in the opcode of a configurable data processing instruction because Trimberger states plainly that "during reconfiguration of the FPGA, the defined execution unit 100 is capable of continuing execution as long as an opcode for the RISA is not encountered." That is, during configuration, the RISA cannot receive an opcode.

In the rejection of the relevant parts of independent Claim 1, the Examiner makes a similar error with the assertion that column 3, lines 31-33 of Trimberger selects the connectivity of operator classes via program instruction opcode. Column 3, lines 30-33 of Trimberger merely states:

> ...A program may reprogram the reprogrammable instruction set accelerator (RISA) several times during the program...

This cited portion of Trimberger does not state that the programming information (configuration code) is provided in a configurable data processing instruction as presently claimed.

In paragraph 20 on page 10 of the Office Action, the Examiner rejects dependent Claim 12, asserting that Trimberger discloses a control map which receives at least one configuration bit from a configurable data processing instruction and provides configuration information to the configurable operators. As explained above, no configuration information is provided in a configurable data processing instruction in Trimberger. Furthermore, no control map is described in Trimberger. The Examiner points to column 7, lines 32-67 of Trimberger which discusses how an opcode is supplied to the RISA. This opcode is associated with a particular configuration of the FPGA which will be

implemented if the current configuration of the FPGA matches the opcode that is supplied. If the opcode does not match the instruction currently programmed into the FPGA, then a reconfiguration operation is required.

There is simply no disclosure of a control map which takes information from a configurable data processing instruction and provides configuration information to the RISA. Trimberger states at column 4, lines 46-50:

> Thus, the reprogrammable instruction set accelerator may be programmed through internal processor data paths or through separate, dedicated programming paths initiated by an instruction from the general purpose, defined execution unit.

Thus, it is a separate activity unconnected with a data processing instruction. The origin of the configuration information is not discussed in Trimberger and certainly there is no suggestion it comes via a control map from the data processing instructions.

In paragraph 22 on page 10 of the Office Action, the Examiner rejects dependent Claim 14, asserting that Trimberger discloses "configuration information controlling interconnectivity from a source other than a configurable data processing information." Trimberger does not disclose configuration "controlling interconnectivity from a source other than a configurable data processing instruction." The RISA of Trimberger only receives operands and opcode from the data processing instruction. (*See, e.g.*, column 7, lines 60-64 where operand data is received at ports A and B and the opcode is supplied at Port I.) The RISA is configured to implement a particular instruction if the current configuration matches the opcode. There is no disclosure of the RISA having a different connectivity such that a source other than a configurable data processing instruction can be used.

In paragraph 23 on page 11 of the Office Action, the Examiner rejects dependent Claim 15, asserting that Trimberger discloses that the execution depth can be greater than two computations, citing column 3, lines 10-27 which disclose a number of operations which can be generally carried out using the RISA. The Examiner asserts these complex functions will take at least two cycles.

The Applicant respectfully wishes to point out that this claim is not directed to the cycle time for a particular activity. The claim relates to the ability of the configuration information to adjust interconnectivity (as stated in Claim 14) such that the result of one operator can be passed directly to another operator without having to go back to a result store and be supplied in a subsequent operation. It is clear from the operation of Trimberger that the RISA will act on a single instruction at a time to provide a result from operands input in an instruction. That result will be returned to a result store and, if needed in a subsequent operation, it would have to be supplied again to the RISA. Furthermore, for that subsequent operation to be implemented, the RISA would have to be reconfigured so as to implement a different instruction.

In paragraph 24 on page 11 of the Office Action, the Examiner rejects dependent Claim 16. Similarly, the Examiner rejects new independent Claim 30. The Examiner asserts that Trimberger discloses a switch mechanism at column 7, lines 45-50. At paragraph d) on page 18 of the Office Action, the Examiner states that when an instruction calls for operation using the configurable operators, operands will be supplied to them. In Trimberger, there is one unit which carries out programmed instructions (RISA) which has a plurality of single-bit operators configured to implement the instruction. There is no possibility in Trimberger to divert operands to any particular part of the FPGA or to any particular operators therein. The RISA is programmed to implement an

instruction on the operands which are provided to it. There seems to be no basis for the comment by the Examiner of:

> For instance, as described above, multipliers may be one group of configurable operators. To perform multiplication, multiple input values (operands) are needed. These operands are therefore switched to the operators for execution.

In Trimberger, operand data is supplied at ports A and B by the RISA and the result data is supplied at port Y. No switching activity whatsoever is discussed within the RISA of Trimberger.

Similarly, referring to the Examiner's rejection in paragraph 25 on page 11 of the Office Action of dependent Claim 17, Trimberger does not disclose the possibility of a feedback loop from the output of the RISA.

For the reasons given in the response of June 10, 2010, incorporated herein in its entirety, the Applicant believes pending independent Claims 1, 22, and 30 are not obvious in view of the cited portions of the cited combination of Trimberger, Haynes, Lodi, and Madurawe, as applied by the Examiner. Furthermore, for the reasons given above, the Applicant believes the limitation of dependent Claim 16, also recited in independent Claim 30, is not obvious in view of the cited combination as applied by the Examiner. Additionally, for the reasons given above, the Applicant believes the limitations in dependent Claims 4-6, 10, 12, 14-15, and 17 are not obvious in view of the cited combination as applied by the Examiner. As such, the cited portions of the cited combination of Trimberger, Haynes, Lodi, and Madurawe, as applied by the Examiner do not provide a *prima facie* case of obviousness for Claims 1-22 and 30. Accordingly, the Applicants respectfully request the Examiner to withdraw the §103(a) rejection of Claims 1-22 and 30 and allow issuance thereof.

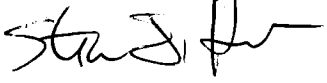
III. Conclusion

In view of the foregoing amendment and remarks, the Applicant respectfully submits that all of the Claims currently pending in this application are in condition for allowance and therefore earnestly solicits a Notice of Allowance for Claims 1-22 and 30.

The Applicant requests the Examiner to telephone the undersigned agent of record at (972) 480-8800 if such would further or expedite the prosecution of the present application. The Commissioner is hereby authorized to charge any fees, credits or overpayments to Deposit Account 08-2395.

Respectfully submitted,

HITT GAINES, PC



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